CLAIMS

1. A semiconductor device utilizing a semiconductor chip, comprising,

a semiconductor chip provided with: a first electrode formed in a small region at a first corner on one surface of a crystal substrate generally quadrangular as viewed in plan; and a second electrode formed in a large region and facing the first electrode, the second electrode being arranged to cover a second corner located diagonally away from the first corner and extend along two sides of the crystal substrate that include the second corner, and

a circuit substrate including an upper surface provided with a pair of external connection electrodes connected to the first electrode and the second electrode via a thermally meltable die-bonding agent such as solder paste,

the external connection electrodes comprising: a first external connection electrode including a first lead connected to the first electrode; and a second external connection electrode including a second lead connected to the second electrode,

the first lead of the first external connection electrode being narrow and extending transversely to one side of the crystal substrate,

the second lead of the second external connection electrode including at least one narrow strip and

extending in a direction opposite to the extending direction of the first lead, the second lead being transverse to another side of the crystal substrate that is generally parallel to said one side to which the first lead is transverse, and

the first lead and the second lead being offset from each other by a prescribed distance.

2. A semiconductor device utilizing a semiconductor chip, comprising,

a semiconductor chip provided with: a first electrode formed in a small region at a first corner on one surface of a crystal substrate generally quadrangular as viewed in plan; and a second electrode formed in a large region and facing the first electrode, the second electrode being arranged to cover a second corner located diagonally away from the first corner and extend along two sides of the crystal substrate that include the second corner, and

a circuit substrate including an upper surface provided with a pair of external connection electrodes connected to the first electrode and the second electrode via a thermally meltable die-bonding agent such as solder paste,

the external connection electrodes comprising: a first external connection electrode including a first lead connected to the first electrode; and a second external connection electrode including a second lead

connected to the second electrode,

the first lead of the first external connection electrode being narrow and extending transversely to one side of the crystal substrate,

the second lead of the second external connection electrode including at least one narrow strip and extending in a direction opposite to the extending direction of the first lead, the second lead being transverse to another side of the crystal substrate that is generally parallel to said one side to which the first lead is transverse, and

the second lead being provided, at an end thereof, with a front electrode piece which is connected to the second electrode and parallel to but offset by a prescribed distance from the first lead.

3. A semiconductor device utilizing a semiconductor chip, comprising,

a semiconductor chip provided with: a first electrode formed in a small region at a central portion along one side on one surface of a crystal substrate generally quadrangular as viewed in plan; and a second electrode formed in a large region and facing the first electrode, the second electrode extending along other three sides of the crystal substrate,

a circuit substrate including an upper surface provided with a pair of external connection electrodes connected to the first electrode and the second electrode

via a thermally meltable die-bonding agent such as solder paste,

the external connection electrodes comprising: a first external connection electrode including a first lead connected to the first electrode; and a second external connection electrode including a second lead connected to the second electrode,

the first lead of the first external connection electrode being narrow and extending transversely to one side of the crystal substrate,

the second lead of the second external connection electrode including at least one narrow strip and extending in a direction opposite to the extending direction of the first lead, the second lead being transverse to another side of the crystal substrate that is generally parallel to said one side to which the first lead is transverse.

4. The semiconductor device utilizing a semiconductor chip according to any one of claims 1-3, wherein the second lead of the second external connection electrode is provided, at an end thereof, with a front electrode piece extending at least in a direction transverse to the longitudinal direction of the second lead and being connected to the second electrode.

5. The semiconductor device utilizing a semiconductor chip according to claim 1 or claim 2, wherein the second

external connection electrode is formed integral with a third lead, and wherein the third lead extends generally in parallel to another side of the crystal substrate that is transverse to the side to which the second lead is transverse, the third lead including an end which is transverse to said another side and connected to the second electrode.

6. The semiconductor device utilizing a semiconductor chip according to claim 5, wherein the first lead, the second lead and the third lead have a width which is about 0.1-0.3 times a length of each of opposing sides of the crystal substrate.

7. The semiconductor device utilizing a semiconductor chip according to any one of claims 1-3, wherein the semiconductor chip comprises a light-emitting element and is at least packaged by a mold made of transparent synthetic resin.

8. The semiconductor device utilizing a semiconductor chip according to any one of claims 1-3, wherein a resist layer is formed on parts of the first, second and third leads, the parts being close to a periphery of the semiconductor chip.